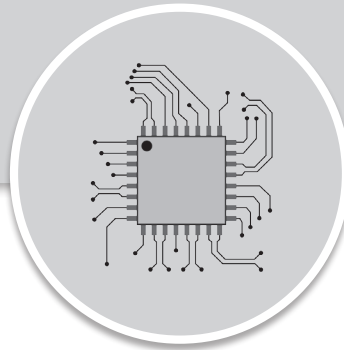


ELECTRONICS ENGINEERING

Computer Organization and Architecture



Comprehensive Theory
with Solved Examples and Practice Questions





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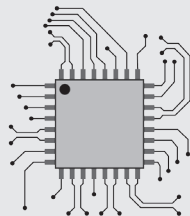
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Computer Organization and Architecture

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EDITIONS

First Edition : 2015
Second Edition : 2016
Third Edition : 2017
Fourth Edition : 2018
Fifth Edition : 2019
Sixth Edition : 2020
Seventh Edition : 2021
Eighth Edition : 2022
Ninth Edition : 2023
Tenth Edition : 2024

Eleventh Edition : 2025

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Computer Organization

1.1 COMPUTER ARCHITECTURE VS COMPUTER ORGANIZATION

Computer Architecture: It is a functional description of requirements and design implementation for the various parts of a computer. It deals with the functional behavior of computer systems. It comes before the computer organization while designing a computer.

Computer Organization: Computer organization is about how operational attributes are linked together and contribute to realizing the architectural specification. Computer organization deals with a structural relationship.

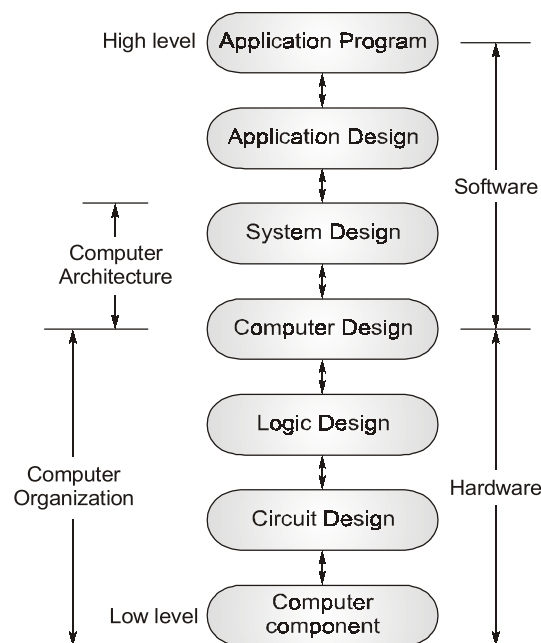


Fig. Computer System



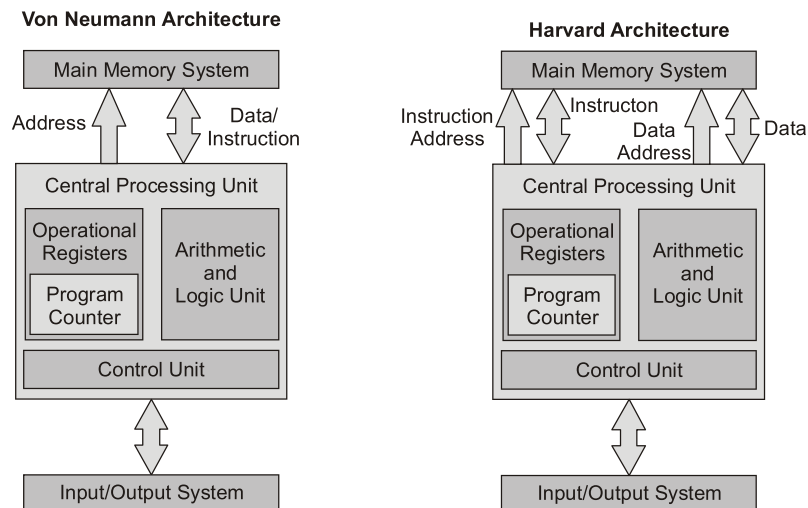
NOTE

Computer architecture describes what the computer does while computer organization describes how the computer does it.

1.1.1 Difference Between Computer Organization and Computer Architecture

Computer Architecture	Computer Organization
<ol style="list-style-type: none"> 1. Computer Architecture deals with the functional behavior of computer system. 2. It deals with high level design issues. 3. Architecture indicates its hardware. 4. It makes the computer's hardware visible. 5. Computer Architecture comprises of logical functions such as instruction sets, registers, data types and addressing modes. 6. Computer Architecture is also called Instruction Set Architecture (ISA). 7. The different architectural categories found in our computer systems are: <ol style="list-style-type: none"> (i) Von-Neumann Architecture (ii) Harvard Architecture (iii) Instruction set architecture (iv) Micro-Architecture (v) System design 	<ol style="list-style-type: none"> 1. Computer organization deals with a structural relationship. 2. It deals with low level design issues. 3. Organization indicates its performance. 4. It offers details on how well the computer performance. 5. Computer organization consists of physical units like circuit designs, peripherals and addresses. 6. Computer organization is frequently called as micro-architecture. 7. CPU organization classified into three categories based on the number of address fields. <ol style="list-style-type: none"> (i) Organization of a single accumulator (ii) Organization of general registers. (iii) Stack organization

1.1.2 Von Neumann Architecture Vs Harvard Architecture



1.2 EVOLUTION OF DIGITAL COMPUTERS

First generation: Vacuum tube computers (1945~1953)

- Program and data reside in the same memory (stored program concepts: John von Neumann)
- Vacuum tubes were used to implement the functions (ALU & CU design)
- Magnetic core and magnetic tape storage devices are used.
- Using electronic vacuum tubes, as the switching components.
- Assembly level language is used

Second generation: Transistorized computers (1954~1965)

- Transistor were used to design ALU & CU
- High Level Language is used (FORTRAN)
- To convert HLL to MLL compiler were used
- Separate I/O processor were developed to operate in parallel with CPU, thus improving the performance
- Invention of the transistor which was faster, smaller and required considerably less power to operate

Third generation: Integrated circuit computers (1965~1980)

- IC technology improved
- Improved IC technology helped in designing low cost, high speed processor and memory modules
- Multiprogramming, pipelining concepts were incorporated
- DOS allowed efficient and coordinate operation of computer system with multiple users
- Cache and virtual memory concepts were developed
- More than one circuit on a single silicon chip became available.

Fourth generation: Very large scale integrated (VLSI) computers (1980~2000)

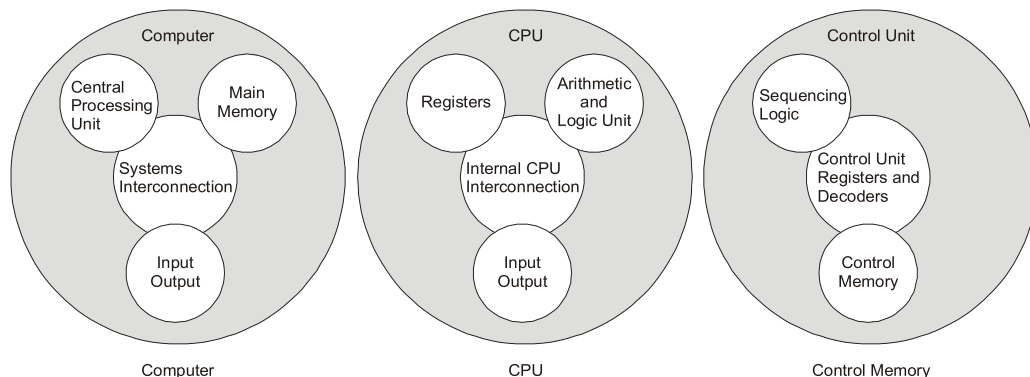
- CPU termed as microprocessor
- INTEL, MOTOROLA, TEXAS, NATIONAL semiconductors started developing microprocessor
- Workstations, microprocessor (PC) & Notebook computers were developed
- Interconnection of different computer for better communication LAN, MAN, WAN
- Computational speed increased by 1000 times
- Specialized processors like Digital Signal Processor were also developed.

Fifth generation: System-on-chip (SOC) computers (2000~)

- E-Commerce, E- banking, home office
- ARM, AMD, INTEL, MOTOROLA
- High speed processor - GHz speed
- Because of submicron IC technology, more features were added in small size.

1.3

COMPONENTS OF COMPUTER STRUCTURE



Computer Structure vs CPU Structure vs Control Unit

1. **Input Unit:** Computers can understand only machine language. Therefore for converting data from human language to machine language we use some special peripheral devices which are called input device.
Examples: Keyboard, Mouse, Joystick, etc.
2. **Output Unit:** After passing instructions for solving particular problem, the results or output from computer is in machine language and this is very difficult to convert that results into human

language. There are several peripheral devices which help us to convert the machine language data into human acceptable data. These devices are called output devices.

Examples: Monitor, Printer, LCD, LED etc.

3. **Memory Unit:** Which is used to store data in computer.

Memory unit performs the following functions

- (a) Stores data and instructions required for processing.
- (b) Stores the intermediate results obtain during processing.
- (c) Stores final results before sending it to output unit.

Two class of storage units: (i) Primary Memory (ii) Secondary Memory

Two types of primary memory are Random Access Memory (RAM) and Read Only Memory (ROM). RAM is used to store data temporarily during the program execution. ROM is used to store data and program which is not going to change.

Secondary Memory is used for bulk storage or mass storage to store data permanently.

4. **CPU:** It is main unit of the computer system. It is responsible for carrying out computational task.

The major structural components of a CPU are:

- (a) **Control Unit (CU):** Controls the operation of the CPU and hence the computer.
- (b) **Arithmetic and Logic Unit (ALU):** Performs computer's data processing functions.
- (c) **Register:** Provides storage internal to the CPU.
- (d) **CPU Interconnection:** communication among the control unit, ALU, and register.

1.4 CISC AND RISC ARCHITECTURES

Complex Instruction Set Computers (CISC)	Reduced Instruction Set Computers (RISC)
• Large instruction set	• Compact instruction set
• Instruction formats are of different lengths	• Instruction formats are all of the same length
• Instructions perform both elementary and complex operations	• Instructions perform elementary operations
• Control unit is microprogrammed	• Control unit is simple and hardwired
• Not pipelined or less pipelined	• Pipelined
• Single register set	• Multiple register set
• Numerous memory addressing options for operands	• Compiler and IC developed simultaneously
• Emphasis on hardware	• Emphasis on software
• Includes multi-clock complex instructions	• Single-clock, reduced instruction only
• Memory-to-memory: "LOAD" and "STORE" incorporated in instructions	• Register to register: "LOAD" and "STORE" are independent instructions
• Small code sizes, high cycles per second	• Low cycles per second, large code sizes
• Transistors used for storing complex instructions	• Spends more transistors on memory registers
Examples of CISC processors: <ul style="list-style-type: none"> • VAX • PDP-11 • Motorola 68000 family • Intel x86 architecture based processors. 	Examples of RISC processors <ul style="list-style-type: none"> • Apple iPods (custom ARM7TDMI SoC) • Apple iPhone (Samsung ARM1176JZF) • Nintendo Game Boy Advance (ARM7) • Sony Network Walkman (Sony in house ARM based chip)

1.5 FLYNN'S CLASSIFICATION OF PROCESSORS

M.J. Flynn offered a classification for a computer systems's organization based on the number of instructions as well as data items that are changed at the same time.

Flynn's classification refers to a classification of parallel computer architectures. Parallel computers can be classified by the concurrency in processing sequences (streams), data, or instructions from the perspective of an assembly language programmer.

Flynn's Classifications are

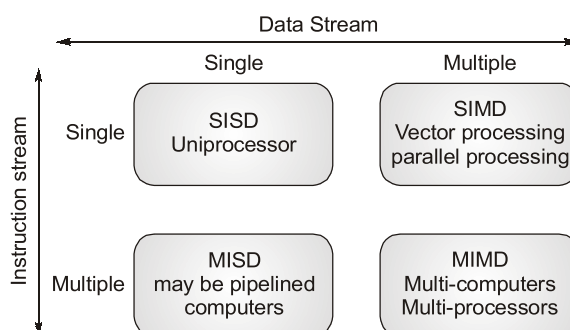
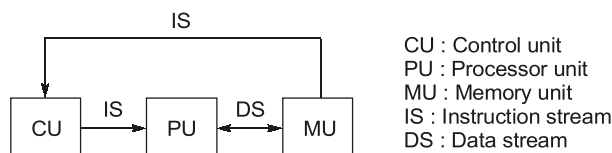


Fig. Flynn's classification of computers

1.5.1 Single Instruction Stream, Single Data Stream (SISD)

A computer with a single processor is called a Single Instruction Stream, Single Data Stream (SISD) Computer. It represents the organization of a single computer containing a control unit, a processor unit, and a memory unit. Instructions are executed sequentially and the system may or may not have internal parallel processing. Parallel processing may be achieved by means of a pipeline processing.

In such a computer a single stream of instructions and a single stream of data are accessed by the processing elements from the main memory, processed and the results are stored back in the main memory. SISD computer organization is shown in figure below.

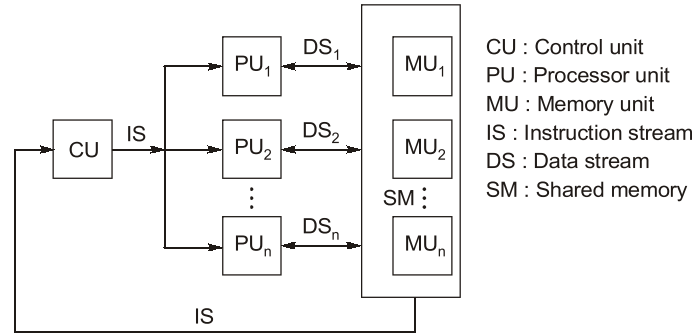


1.5.2 Single Instruction Stream, Multiple Data Stream (SIMD)

It represents an organization of computer which has multiple processors under the supervision of a common control unit. All processors receive the same instruction from the control unit but operate on different items of the data. SIMD computers are used to solve many problems in science which require identical operations to be applied

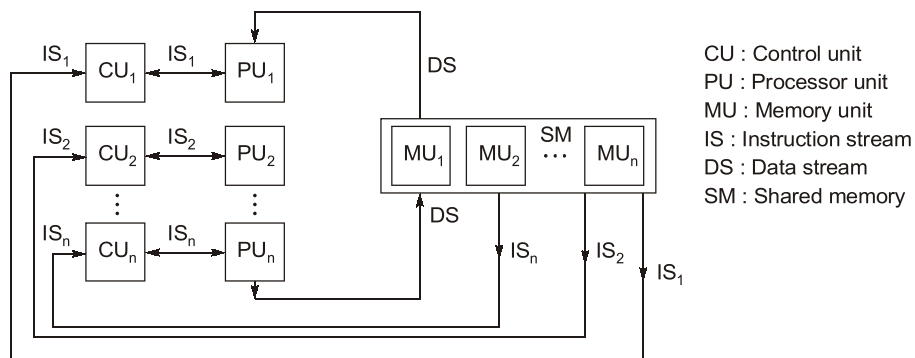
to different data set synchronously. Examples are adding a set of matrices simultaneously, such as $\sum_i \sum_k (a_{ik} + a_{ik})$.

Such computers are known as array processors. SIMD computer organization is shown in figure below.



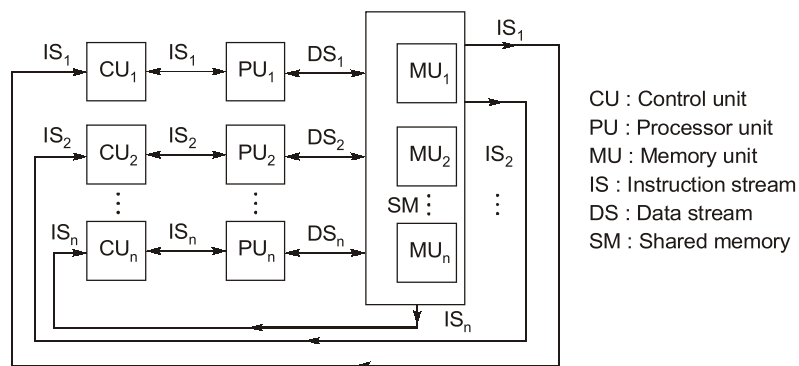
1.5.3 Multiple Instruction Stream, Single Data Stream (MISD)

It refers to the computer in which several instructions manipulate the same data stream concurrently. In this structure different processing element run different programs on the same data. This type of processor may be generalized using a 2-dimensional arrangement of processing element. Such a structure is known as systolic processor. MISD computer organization is shown in figure below.



1.5.4 Multiple Instruction Stream, Multiple Data Stream (MIMD)

MIMD computers are the general purpose parallel computers. Its organization refers to a computer system capable of processing several programs at a same time. MIMD systems include all multiprocessing systems. MIMD computer organization is shown in figure below.]



1.13.9 Optimal Replacement Algorithm

The optimal replacement algorithm is used to reduce the page faults. It uses the principle that "When a page is called by the system and it is not available in the frames, the frame which is not in demand for the longest future time is replaced by the new page".

EXAMPLE : 1.25

Assume there are 4 frames, and consider the following reference string. Find the number of page faults using optimal page replacement algorithm.

7, 0, 1, 2, 0, 3, 0, 4, 2, 3, 0, 3, 2, 3

Solution :

7	0	1	2	0	3	0	4	2	3	0	3	2	3
7	7	7	7	7	3	3	3	3	3	3	3	3	3
	0	0	0	0	0	0	0	0	0	0	0	0	0
		1	1	1	1	1	4	4	4	4	4	4	4
			2	2	2	2	2	2	2	2	2	2	2
X	X	X	X		X		X						

Number of page fault = 6.

SUMMARY

- **Computer:** A device that accepts input, processes data, stores data, and produces output, all according to a series of stored instructions.
- **Hardware:** Includes the electronic and mechanical devices that process the data; refers to the computer as well as peripheral devices.
- **Software:** A computer program that tells the computer how to perform particular tasks.
- **Computer organization:** Interconnection of hardware to form the computer system
- **Computer architecture:** the structure and behaviour of the computer perceived by the user.
- **Input:** The data or raw information entered into a computer.
- **Data:** Refers to the symbols that represent facts, objects, or ideas.
- **Information:** The results of the computer storing data as bits and bytes; the words, numbers, sounds, and graphics.
- **Output:** Consists of the processing results produced by a computer.
- **Main Memory:** Area of the computer that temporarily holds data waiting to be processed, stored, or output. *Example:* Cache and Main memory
- **Secondary Storage:** Area of the computer that holds data on a permanent basis when it is not immediately needed for processing. *Example:* Disk, Floppy, etc.



**OBJECTIVE
BRAIN TEASERS**

- Q.1** What does CISC and RISC means?
(a) common instruction set controller and rare instruction set controller
(b) complex instruction set controller and reduced instruction set controller
(c) compiled instruction set source code and recompiled instruction source code
(d) none of the above
- Q.2** A 32-bit address bus allows access to a memory of capacity
(a) 64 Mb (b) 16 Mb
(c) 1 Gb (d) 4 Gb
- Q.3** The system bus is made up of
(a) data bus
(b) data bus and address bus
(c) data bus and control bus
(d) data bus, control bus and address bus
- Q.4** Which of the following is not involved in a memory write operation?
(a) MAR (b) PC
(c) MDR (d) data bus
- Q.5** The read/write line
(a) belongs to the data bus
(b) belongs to the control bus
(c) belongs to the address bus
(d) CPU bus
- Q.6** _____ is a piece of hardware that executes a set of machine-language instructions.
(a) controller (b) bus
(c) processor (d) motherboard
- Q.7** Given below are some statements associated with the registers of a CPU. Identify the false statement.
(a) The program counter holds the memory address of the instruction in execution.
(b) Only opcode is transferred to the control unit.
(c) An instruction in the instruction register consists of the opcode and the operand.
(d) The value of the program counter is incremented by 1 once its value has been read to the memory address register.
- Q.8** The following are four statements regarding what a CPU with only a set of 32 bit registers can perform.
1. Hold and operate on 32 bit integers
2. Hold and operate on 16 bit integers
3. Hold and operate on 64 bit floating point arithmetic
4. Hold and operate on 16 bit UNICODE characters
Which of the following is true about such a CPU?
(a) all are true (b) 1,2 and 3 only
(c) 1,2 and 4 only (d) 1,3 and 4 only
- Q.9** The following are four statements about Reduced Instruction Set Computer (RISC) architectures.
1. The typical RISC machine instruction set is small, and is usually a subset of a CISC instruction set.
2. No arithmetic or logical instruction can refer to the memory directly.
3. A comparatively large number of user registers are available.
4. Instructions can be easily decoded through hard-wired control units.
Which of the above statements is true?
(a) 1 and 3 only (b) 1,3 and 4 only
(c) 1, 2 and 3 only (d) All of these
- Q.10** The word length of a CPU is defined as
(a) the maximum addressable memory size
(b) the width of a CPU register (integer or float point)
(c) the width of the address bus
(d) the number of general purpose CPU registers
- Q.11** Which of the following statements is false about CISC architectures?
(a) CISC machine instructions may include complex addressing modes, which require many clock cycles to carry out.
(b) CISC control units are typically micro-programmed, allowing the instruction set to be more flexible.
(c) In the CISC instruction set, all arithmetic/logic instructions must be register based.
(d) CISC architectures may perform better in network centric applications than RISC.

- Q.12** What will be average cost per bit for a system with main memory of 1024 cost, 100 units and secondary memory of 4096 cost, 10 units.
 (a) 35.7 (b) 28.0
 (c) 82.0 (d) insufficient data
- Q.13** Consider a Disk I/O transfer, in which 1500 bytes are to be transferred, but number of bytes on a track is 1000, and rotation speed of disk is 1500 rps but the average time required to move the disk arm to the required track is 15 ms, then what will be total access time?
 (a) 16.33 ms (b) 15.33 ms
 (c) 16.33 μ s (d) 15.33 μ s
- Q.14** A disc drive has a rotational speed of 3600 rpm, an average seek time of 10 ms, 64 sectors per track and 512 bytes of data per sector. What is the average time to access the entire data of a 16 kbytes file stored sequentially on the disk?
 (a) 18.85 ms (b) 10 ms
 (c) 26.67 ms (d) 9 ms
- Q.15** The seek time of a disk is 30 msec. It rotates at the rate of 30 rotations per second. Each track has a capacity of 300 words. The access time is
 (a) 47 msec (b) 50 msec
 (c) 60 msec (d) 62 msec
- Q.16** A disc rotates at a speed of 7200 rpm. It has 4000 cylinders, 16 surfaces and 256 sectors per track. What is the average latency time of the disk?
 (a) 8.33 ms (b) 4.166 ms
 (c) 41.66 ms (d) 83.3 ms
- Q.17** A magnetic drum of 8 inch diameter has 100 tracks and storage density of 200 bits/inch. What is its storage capacity?
 (a) 8402 bits (b) 202400 bits
 (c) 502400 bits (d) 1004800 bits
- Q.18** Which of the following affects processing power?
 (a) data bus capacity
 (b) addressing scheme
 (c) clock speed
 (d) all of the above

- Q.19** A _____ is required to translate such microprogram into executable programs that can be stored in the control memory in microprogramming.
 (a) microassembler
 (b) microcompiler
 (c) microprogrammed CPU
 (d) microprogrammed counter

ANSWERS KEY

1. (d) 2. (d) 3. (d) 4. (b) 5. (b)
 6. (c) 7. (a) 8. (c) 9. (d) 10. (b)
 11. (c) 12. (b) 13. (a) 14. (c) 15. (b)
 16. (b) 17. (c) 18. (d) 19. (a)

HINTS & EXPLANATIONS**1. (d)**

CISC : Complex Instruction Set Architecture.
 RISC : Reduced Instruction Set Architecture.

2. (d)

Address bus size = 32 bit
 Capacity of memory = 2^{32} b
 $= 4 \times 2^{30}$ b
 $= 4$ Gb

4. (b)

Program counter (PC) register used to read the value or instruction not in write operation. For write operation MAR, IR and MDR registers are used.

5. (b)

The read/write line belongs to control bus:
 Read (\overline{RD}), write (\overline{WR}) and byte enable (\overline{E}).

6. (c)

Processor or processing unit is used to perform operations on some external source, usually memory or some data stream, processor executes a set of machine language instructions.

7. (a)

The program centre (PC) holds the memory address of the next instruction to be executed, whereas, the address of the instruction in execution is stored in Memory Address Register (MAR).

8. (c)

A CPU with only a set of 32-bit registers can perform:

- Hold and operate on 32-bit integers.
- Hold and operate on 16-bit integers.
- Hold and operate on 16-bit UNICODE characters.

10. (b)

The word length of a CPU is defined as the width of a CPU register i.e. at a time number of instructions process by the processor.

11. (c)

In the RISC instruction set, all arithmetic/logic instructions must be register based.

12. (b)

Total cost for 1024 of main memory is 100 units.
Total cost for 4096 bits of secondary memory is 10 units.

$$\begin{aligned}\text{Average cost per bit} &= \frac{\text{Total cost of the system}}{\text{Total number of bits}} \\ &= \frac{1024 \times 100 + 4096 \times 10}{1024 + 4096} = 28\end{aligned}$$

13. (a)

Given,

$$\text{Seek time} = 15 \text{ ms}$$

$$\text{Average rotational latency} = \frac{1}{2} \times \text{rotation time}$$

$$\begin{aligned}\text{Rotation time} &= \frac{1}{1500} \text{ sec} = 0.667 \text{ msec} \\ \text{to transfer 1500 bytes of data is requires}\end{aligned}$$

$$\frac{1500}{1500 \times 1000} = 1 \text{ msec}$$

$$\text{Total average time} = (\text{Seek time}) + (\text{Average rotational latency}) + \text{Transfer time}$$

$$\text{Total average time} = 15 + \frac{0.67}{2} + 1 = 16.33 \text{ ms}$$

14. (c)

Given,

$$\text{Average seek time} = 10 \text{ ms}$$

$$\text{Rotational speed} = 3600 \text{ rpm}$$

$$\text{Total capacity of each track} = 64 \times 512 = 32 \text{ kB}$$

$$\text{Average rotational latency} = \frac{1 \times 60}{2 \times 3600} = 8.33 \text{ s}$$

$$1 \text{ B data transfer time} = \frac{16.667}{32k} \text{ ms}$$

$$\begin{aligned}16 \text{ kB data transfer time} \\ &= \frac{16.667}{32k} \times 16k = 8.33 \text{ ms}\end{aligned}$$

$$\begin{aligned}\text{Average access time} &= 10 + 8.33 + 8.33 \\ &= 26.66 \text{ ms}\end{aligned}$$

15. (a)

$$\text{Seek time} = 30 \text{ ms}$$

$$1 \text{ rotation time} = \frac{1}{30} \text{ sec}$$

Average rotational latency

$$= \frac{1}{2} \times \frac{1}{30} = 16.67 \text{ ms}$$

$$300 \text{ word requires } \frac{1}{30} \text{ sec}$$

$$1 \text{ word requires } \frac{1}{30} \times \frac{1}{30} \text{ sec} = 0.11 \text{ ms}$$

$$\begin{aligned}\text{Average access time} \\ &= 30 + 16.67 + 0.11 = 46.78 \text{ ms}\end{aligned}$$

16. (b)

$$\text{Rotational speed} = 7200 \text{ rpm}$$

Average rotation latency

$$= \frac{1}{2} \times \frac{1}{7200} \times 60 = 4.167 \text{ ms}$$

17. (c)

$$\text{Diameter} = 8 \text{ inch}$$

$$\text{No. of tracks} = 100$$

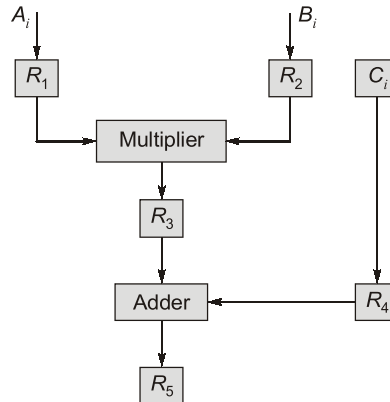
$$\text{Storage density} = 200 \text{ bits/inch}$$

$$\begin{aligned}\text{Storage capacity} &= \pi \times 8 \times 100 \times 200 \\ &\approx 502400 \text{ bits}\end{aligned}$$



CONVENTIONAL BRAIN TEASERS

- Q.1** The pipeline of figure shown has the following propagation times: 40 nsec for the operands to be read from memory into registers R_1 and R_2 , 45 nsec for the signal to propagate through the multiplier, 5 nsec for the transfer into R_3 and 15 nsec to add the two numbers into R_5 .



- (i) What is the minimum clock cycle time that can be used?
- (ii) A non-pipeline system can perform the same operation by removing R_3 and R_4 . How long will it take to multiply and add the operands without using the pipeline?
- (iii) Calculate the speedup that can be achieved with pipeline for 10 tasks.
- (iv) What is the maximum speed up that can be achieved?

1. (Sol.)

- (i) This pipeline shows combined operation:

$$A_i \times B_i + C_i$$

The operations performed can be grouped into 3 segments each performing a suboperation as shown:

S-1 $R_1 \leftarrow A_i ; R_2 \leftarrow B_i$

S-2 $R_3 \leftarrow R_1 \times R_2 ; R_4 \leftarrow C_i$

S-3 $R_5 \leftarrow R_3 + R_4$

$\therefore K = 3$

Segment 1 takes = 40 nsec

Segment 2 takes = 45 + 5 = 50 nsec

Segment 3 takes = 15 nsec

$$\begin{aligned} \therefore \text{Minimum clock cycle time} &= \text{Max (Seg1, Seg2, Seg3)} \\ &= \text{Max}[40, 50, 15] \\ &= 50 \text{ nsec} \end{aligned}$$

- (ii) Without pipeline

$$t_n = 40 + 45 + 15 = 100 \text{ nsec}$$

\therefore If there is no pipeline, then it will take 100 nsec.

(iii) Speedup for n tasks

$$S = \frac{n \times t_n}{[K + (n-1)]t_p}$$

\therefore For $n = 10$,

$$S = \frac{10 \times 100}{(3+9) \times 50} = 1.67$$

(iv) Maximum speedup

$$\Rightarrow S_{\max} = \frac{t_n}{t_p} = \frac{100}{50} = 2$$

Q.2 A single-level paging scheme using TLB. TLB access time is 10 nsec and main memory access time is 50 nsec. What is the effective memory access time if TLB hit ratio is 90% and there is no page fault?

2. (Sol.)

Given data,

$$T_m = 50 \text{ nsec}$$

$$T_{TLB} = 10 \text{ nsec}$$

$$H = 90\% = 0.9$$

\therefore Effective memory access time

$$EMAT = \text{Hit Ratio [TLB + MM]} + \text{Miss [TLB + 2MM]}$$

$$= 0.9[10 + 50] + 0.1[10 + 100] = 54 + 11$$

$$EMAT = 65 \text{ nsec}$$

Q.3 Assume that the main memory has 3 page frames, and consider the following page reference string. Find the number of page faults using FIFO, optimal (MIN) and LRU page replacement algorithm.

7, 0, 1, 2, 0, 3, 0, 4, 2, 3, 0, 3, 2, 1, 2, 0, 1, 7, 0, 1

3. (Sol.)

FIFO:

	7	0	1	2	0	3	0	4	2	3	0	3	2	1	2	0	1	7	0	1
0	7	7	7	2	2	2	2	4	4	4	0	0	0	0	0	①	0	7	7	7
1		0	0	0	①	3	3	3	2	2	2	2	②	1	1	1	①	1	0	0
2			1	1	1	1	0	0	0	3	3	③	3	3	2	2	2	2	2	1

* * * *

Total page hits = 5

Total page faults = 20 – 5 = 15

Optimal (Min):

	7	0	1	2	0	3	0	4	2	3	0	3	2	1	2	0	1	7	0	1
0	7	7	7	2	2	2	2	2	②	2	2	2	②	2	②	2	2	7	7	7
1		0	0	0	①	0	①	4	4	4	0	0	0	0	0	①	0	0	①	0
2			1	1	1	3	3	3	3	③	3	③	3	1	1	1	①	1	1	①

* * * * *

Total Page hits = 11

Total page faults = 20 – 11 = 9